8089
I/O Processor
iAPX86 Family

DISTINCTIVE CHARACTERISTICS

- High speed DMA capability
- Two DMA channels
- Removes I/O software overhead from 8086/8088
- 1 megabyte addressability
- 1.25 Mbyte/sec transfer rate
- Memory-based communication with CPU
- Allows mixed interface of 8- and 16-bit peripherals
- LOCAL or REMOTE I/O processing modes
- Multibus compatible system interface

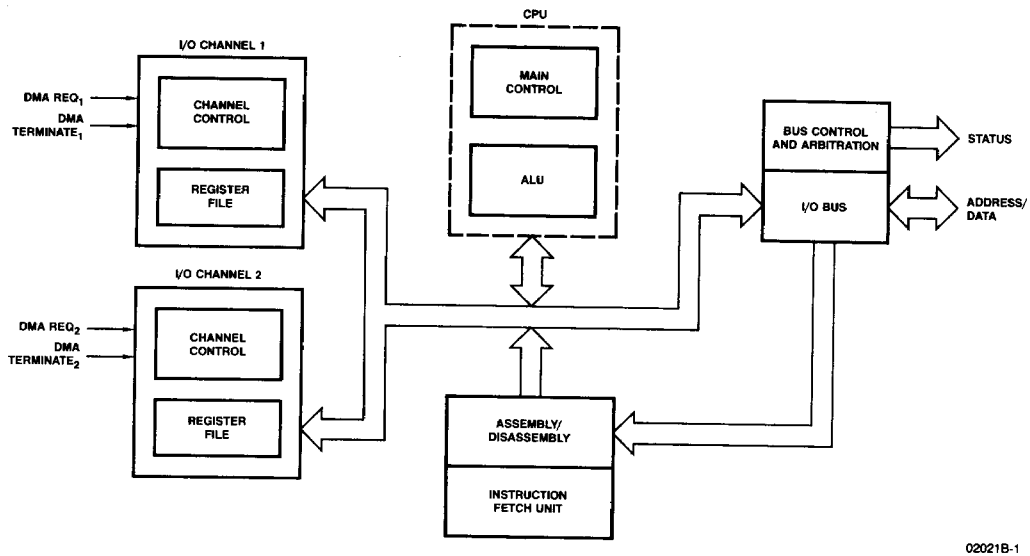
GENERAL DESCRIPTION

The 8089 is a high performance I/O processor designed for the 8086 Family. It supports versatile DMA functions and maintains peripheral components, to offload I/O overhead from the CPU. The IOP communicates with the CPU through shared memory blocks and 2 control lines.

The 8089 IOP can operate in LOCAL mode sharing the same bus and buffer with the CPU, or in REMOTE mode on a separate local bus. In REMOTE mode the 8089 is compatible with any 8080 or 8085 CPU as well.

The 8089 IOP is particularly effective in I/O intensive applications like filter and buffer management, CRT control, and other communications tasks. It is implemented in N-channel depletion load silicon, packaged in a 40-pin DIP.

BLOCK DIAGRAM



ORDERING INFORMATION

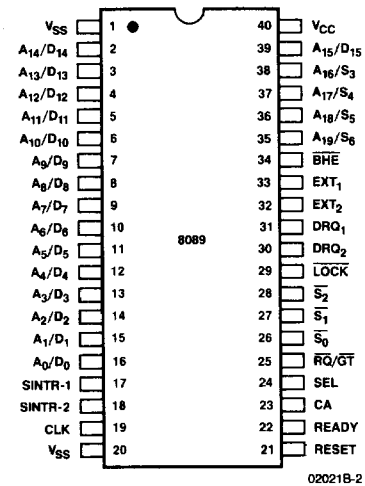
Package Type	Ambient Temperature Spec	Order Number
Hermetic Dip	$0°C \leq T_A \leq 70°C$	D8089-3

Multibus is a trademark of Intel Corp.

TABLE 1. PIN DESCRIPTION

Symbol	Type	Name and Function
A_0-A_{15}/ D_0-D_{15}	I/O	**Multiplexed Address and Data Bus:** The function of these lines are defined by the state of $\overline{S}_0$, $\overline{S}_1$ and $\overline{S}_2$ lines.
A_{16}-A_{19}/ S_3-S_6	O	**Address and Status:** Multiplexed most significant address lines and status information. The address lines are active only when addressing memory. Otherwise, the status lines are active.
$\overline{BHE}$	O	**Bus High Enable:** The Bus High Enable is used to enable data operations on the most significant half of the data bus (D_8-D_{15}).
$\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$	O	**Status:** These are the status pins that define the IOP activity during any given cycle. The status lines are utilized by the bus controller and bus arbiter to generate all memory and I/O control signals.
READY	I	**Ready:** The ready signal received from the addressed device indicates that the device is ready for data transfer.
$\overline{LOCK}$	O	**Lock:** The lock output signal indicates to the bus controller that the bus is needed for more than one contiguous cycle.
RESET	I	**Reset:** The receipt of a reset signal causes the IOP to suspend all its activities and enter an idle state until a channel attention is received.
CLK	I	**Clock:** Clock provides all timing needed for internal IOP operation.
CA	I	**Channel Attention:** Gets the attention of the IOP
SEL	I	**Select:** The first CA received after system reset informs the IOP via the SEL line, whether it is a Master or Slave and starts the initialization sequence.
DRQ1-2	I	**Data Request:** DMA request inputs which signal the IOP that a peripheral is ready to transfer/receive data.
$\overline{RQ}/\overline{GT}$	I/O	**Request Grant:** Request Grant implements the communication dialogue required to arbitrate the use of the system bus or I/O bus.
SINTR1-2	O	**Signal Interrupt:** Signal Interrupt outputs from channels 1 and 2 respectively.
EXT1-2	I	**External Terminate:** External terminate inputs for channels 1 and 2 respectively.
V_{CC}		**Voltage:** +5 volt power input.
V_{SS}		**Ground.**

CONNECTION DIAGRAM
Top View
D-40



Note: Pin 1 is marked for orientation.

OPERATING MODES

Shown in Figure 3 is the 8089 in a LOCAL configuration. The 8086/88 CPU is used in its maximum mode. The 8089 and CPU reside on the same local bus, sharing the same set of system buffers. Peripherals located on the system bus can be addressed by either the CPU or the 8089. The 8089 requests the use of the LOCAL bus by means of the RQ/GT line. When the CPU relinquishes the system bus, the 8089 uses the same bus control, latches and transceiver components to generate the system address, control and data lines.

A typical REMOTE configuration is shown in Figure 4. In this mode, the IOP's bus is physically separated from the system bus by means of system buffers/latches. The IOP maintains its own local bus and can operate out of local or system memory. The system bus interface contains the following components: 8282 latches, 8286 transceiver, 8288 bus controller, and 8283 bus arbiter.

The peripheral devices PER_1 and PER_2 are supported on their own data and address bus. The 8089 communicates with the peripherals without affecting system bus operation. Optional buffers may be used on the local bus when capacitive loading conditions so dictate.

COMMUNICATION MECHANISM

Communication between the CPU and IOP is performed through messages prepared in shared memory. The CPU can cause the 8089 to execute a program by placing it in the 8089's memory space and/or directing the 8089's attention to it by asserting a hardware Channel Attention (CA) signal to the IOP, activating the proper I/O channel. Communication from the IOP to the processor can be performed in a similar manner via a system interrupt (SINTR 1, 2), if the CPU has enabled interrupts for this purpose.

The Control Block furnishes bus control initialization for the IOP operation (CCW or Channel Control Word) and provides pointers to the Parameter Block or "data" memory for both channels 1 and 2.

The Parameter Block contains the address of the Task Block and acts as a message center between the IOP and CPU. Parameters or variable information is passed from the CPU to its IOP in this block to customize the software interface to the peripheral device. It is also used for transferring data and status information between the IOP and CPU.

The Task Block contains the instructions for the respective channel. This block can reside on the local bus of the IOP, allowing the IOP to operate concurrently with the CPU, or reside in system memory.

Register Set

The 8089 maintains separate registers for its two I/O channels as well as some common registers (see Figure 6). There are sufficient registers for each channel to sustain its own DMA transfers, and process its own instruction stream.

Bus Operation

The 8089 utilizes the same bus structure as the 8086 and 8088 in their maximum mode configurations (see Figure 7).

The data bandwidth of the IOP is a function of the physical bus width of the system and I/O busses. Table 2 gives the bandwidth, latency and bus utilization of the 8089. The system bus is assumed to be 16-bits wide with either an 8-bit peripheral (under byte column) or 16-bit peripheral (word column) being shown.

The latency refers to the worst case response time by the IOP to a DMA request, without the bus arbitration times. Notice that the word transfer allows 50% more bandwidth. This occurs since three bus cycles are required to map 8-bit data into a 16-bit location, versus two for a 16-bit to 16-bit transfer. Note that it is possible to fully saturate the system bus in the LOCAL mode whereas in the REMOTE mode this is reduced to a maximum of 50%.

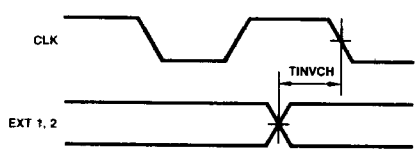
TABLE 2. ACHIEVABLE 5MHz 8089 OPERATIONS

	Local		Remote	
	Byte	**Word**	**Byte**	**Word**
Bandwidth	830 KB/S	1250 KB/S	830 KB/S	1250 KB/S
Latency	1.0/2.4 μsec*	1.0/2.4 μsec*	1.0/2.4 μsec*	1.0/2.4 μsec*
System Bus Utilization	2.4μsec Per Transfer	1.6μsec Per Transfer	0.8μsec Per Transfer	0.8μsec Per Transfer

*2.4μsec if interleaving with other channel and no wait states. 1μsec if channel is waiting for request.

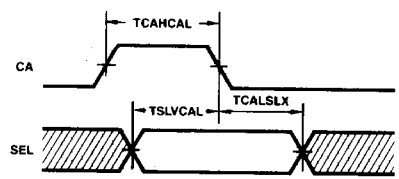
WAVEFORMS

EXTERNAL TERMINATE SETUP



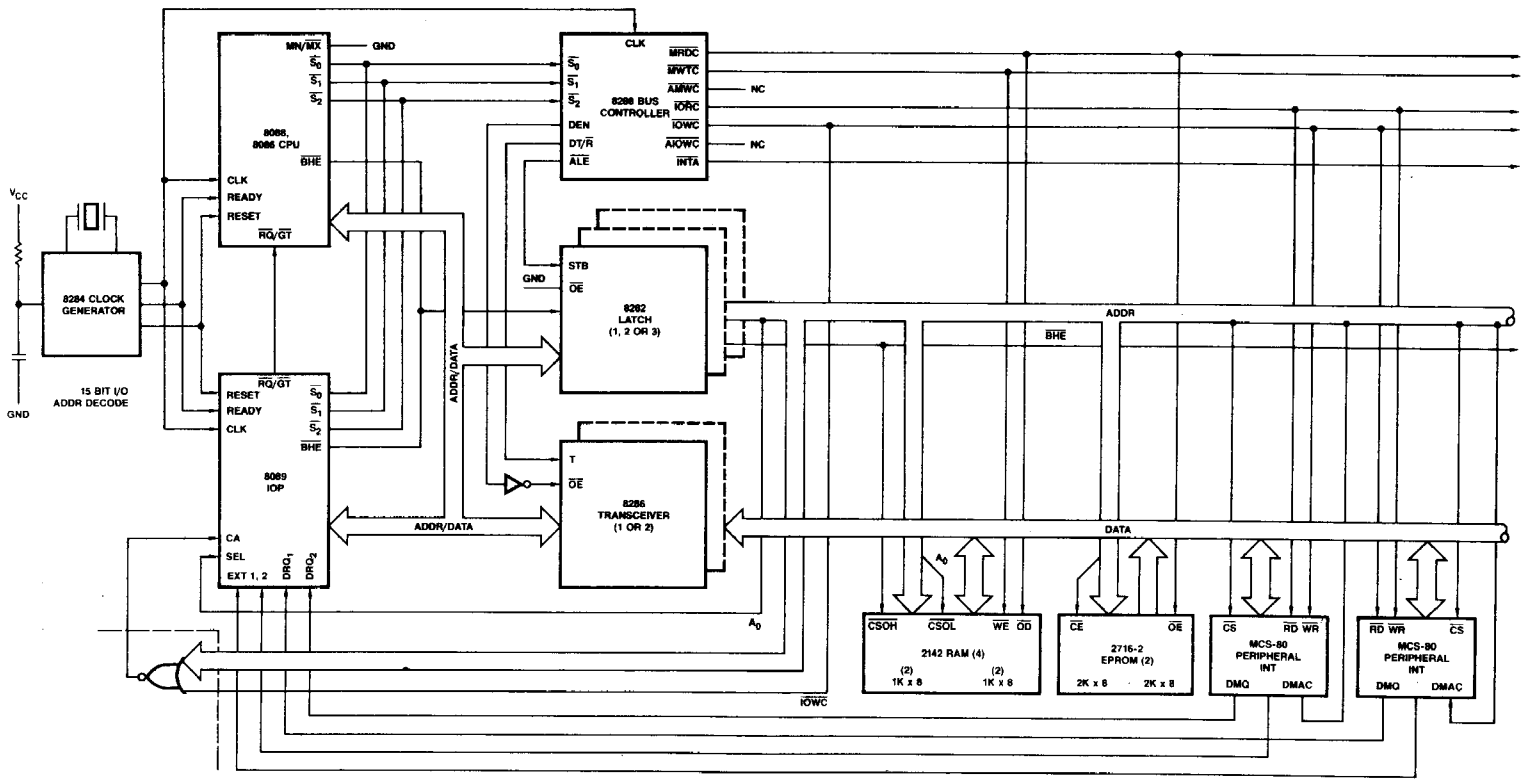
02021B-15

SEL SETUP AND TIMING



02021B-16

Figure 3. Typical Configuration with 8089 in LOCAL Mode, 8088, 8086 in MAX Mode



Note: Only one latch is needed if configured with 8086 and only 64K addressing is used. Only one transceiver is needed if using a physical 8-bit data bus (8088).

Figure 4. Typical REMOTE Configuration

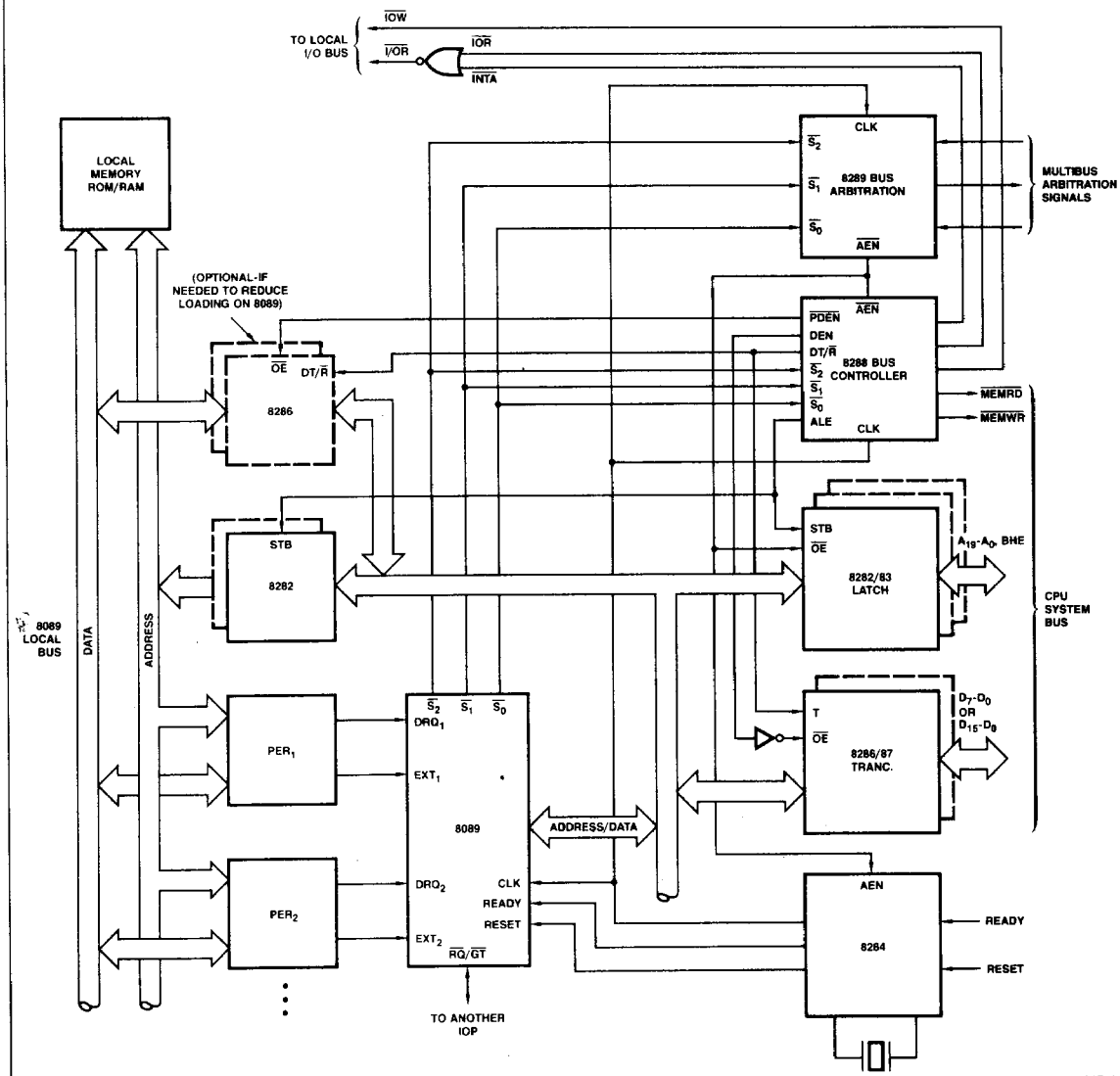


Figure 5. Communication Data Structure Hierarchy

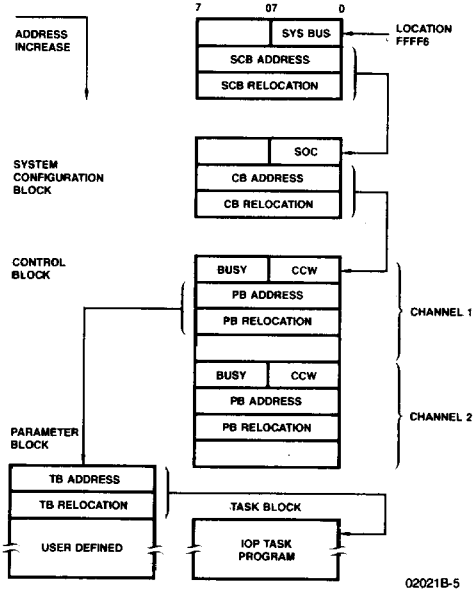


Figure 6. Register Model

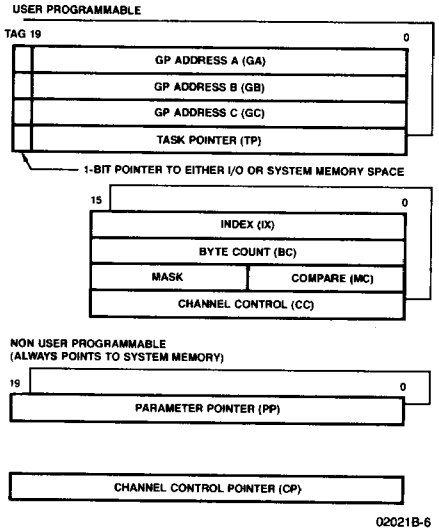
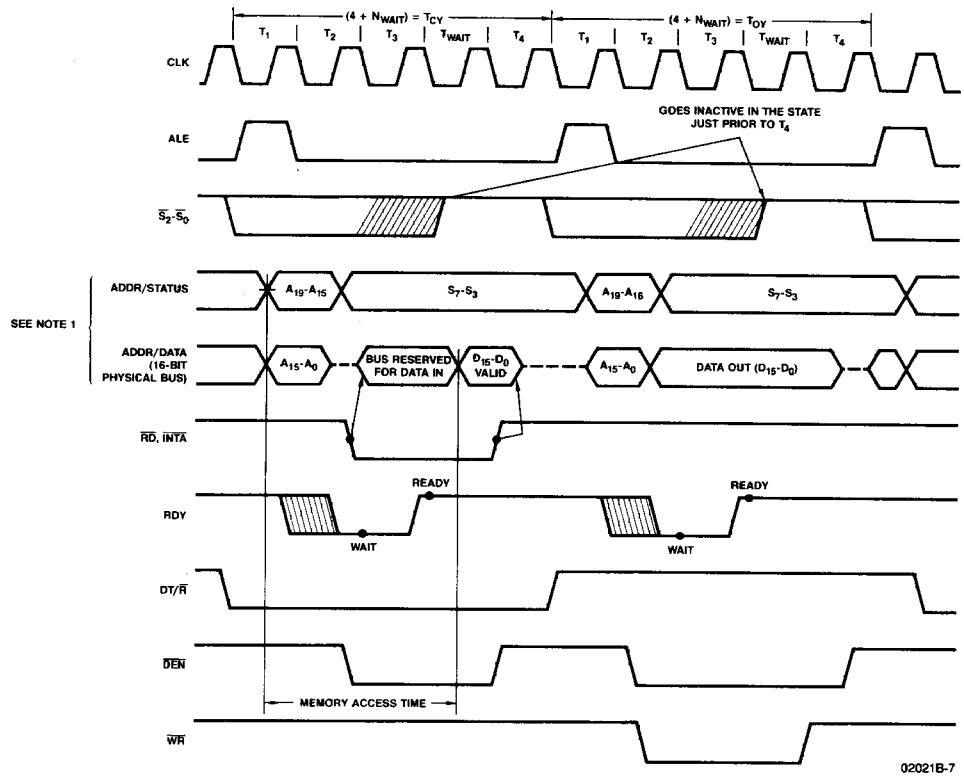


Figure 7. 8089 Bus Operation



Note: 1. BHE is stable (i.e., non multiplexed) throughout each transfer cycle. A_8-A_{15} are also stable on transfers to a physical 8-bit bus.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0 to 70°C
Storage Temperature	−65 to +150°C
Voltage on Any Pin with Respect to Ground	−1.0 to +7V
Power Dissipation	2.5 Watt

*Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = 5V ±10%)

Parameter	Description	Test Conditions	Min	Max	Units
V_{IL}	Input Low Voltage		−0.5	+0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} +1.0	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −400μA	2.4		V
I_{CC}	Power Supply Current	T_A = 25°C		350	mA
I_{LI}	Input Leakage Current (See Note 1)	0V < V_{IN} < V_{CC}		±10	μA
I_{LO}	Output Leakage Current	0.45V ≤ V_{OUT} ≤ V_{CC}		±10	μA
V_{CL}	Clock Input Low Voltage		−0.5	+0.6	V
V_{CH}	Clock Input High Voltage		3.9	V_{CC} +1.0	V
C_{IN}	Capacitance of Input Buffer (All input except AD_0-AD_{15}, $\overline{RQ}/\overline{GT}$)	fc = 1MHz		15	pF
C_{IO}	Capacitance of I/O Buffer (AD_0-AD_{15}, $\overline{RQ}/\overline{GT}$)	fc = 1MHz		15	pF

AC CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = 5V ±10%)

8089/8086 MAX MODE SYSTEM (USING 8288 BUS CONTROLLER) TIMING REQUIREMENTS

Parameter	Description	Test Conditions	Min	Max	Units
TCLCL	CLK Cycle Period		200	500	ns
TCLCH	CLK Low Time		(2/3 TCLCL) −15		ns
TCHCL	CLK High Time		(1/3 TCLCL) +2		ns
TCH1CH2	CLK Rise Time	From 1.0 to 3.5V		10	ns
TCL2CL1	CLK Fall Time	From 3.5 to 1.0V		10	ns
TDVCL	Data In Setup Time		30		ns
TCLDX	Data In Hold Time		10		ns
TR1VCL	RDY Setup Time into 8284 (See Notes 1, 2)		35		ns
TCLR1X	RDY Hold Time into 8284 (See Notes 1, 2)		0		ns
TRYHCH	READY Setup Time into 8089		(2/3 TCLCL) −15		ns
TCHRYX	READY Hold Time into 8089		30		ns
TRYLCL	READY Inactive to CLK (See Note 4)		−8		ns
TINVCH	Setup Time Recognition (DRQ 1, 2 RESET, Ext 1, 2) (See Note 2)		30		ns
TGVCH	$\overline{RQ}/\overline{GT}$ Setup Time		30		ns
TCAHCAL	CA Width		95		ns
TSLVCAL	SEL Setup Time		75		ns
TCALSLX	SEL Hold Time		0		ns
TCHGX	GT Hold Time into 8089		40		ns
TILIH	Input Rise Time (Except CLK)	From 0.8 to 2.0V		20	ns
TIHIL	Input Fall Time (Except CLK)	From 2.0 to 0.8V		12	ns

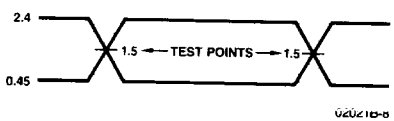
AC CHARACTERISTICS (Cont.) (T_A = 0 to 70°C, V_{CC} = 5V ±10%)

TIMING RESPONSES

Parameter	Description	Test Conditions	Min	Max	Units
TCLML	Command Active Delay (See Note 1)	C_L = 80pF	10	35	ns
TCLMH	Command Inactive Delay (See Note 1)		10	35	ns
TRYHSH	READY Active to Status Passive (See Note 3)			110	ns
TCHSV	Status Active Delay		10	110	ns
TCLSH	Status Inactive Delay		10	130	ns
TCLAV	Address Valid Delay		10	110	ns
TCLAX	Address Hold Time		10		ns
TCLAZ	Address Float Delay		TCLAX	80	ns
TSVLH	Status Valid to ALE High (See Note 1)	C_L = 150pF		15	ns
TCLLH	CLK Low to ALE Valid (See Note 1)			15	ns
TCHLL	ALE Inactive Delay (See Note 1)			15	ns
TCLDV	Data Valid Delay		10	110	ns
TCHDX	Data Hold Time		10		ns
TCVNV	Control Active Delay (See Note 1)		5	45	ns
TCVNX	Control Inactive Delay (See Note 1)		10	45	ns
TCHDTL	Direction Control Active Delay (See Note 1)			50	ns
TCHDTH	Direction Control Inactive Delay (See Note 1)			30	ns
TCLGL	$\overline{RQ}$ Active Delay	C_L = 100pF	0	85	ns
TCLGH	$\overline{RQ}$ Inactive Delay	Note 5: C_L = 30pF		85	ns
TCLSRV	SINTR Valid Delay	C_L = 100pF		150	ns
TOLOH	Output Rise Time	From 0.8 to 2.0V		20	ns
TOHOL	Output Fall Time	From 2.0 to 0.8V		12	ns

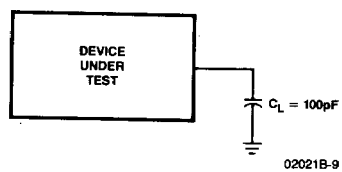
Notes: 1. Signal at 8284 or 8288 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T_3 and T_W states.
4. Applies only to T_2 state.
5. Applies only if RQ/GT mode 1 C_L = 30pF, 2.7kΩ pull up to V_{CC}.

AC TESTING INPUT, OUTPUT WAVEFORM



AC testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0." The clock is driven at 4.3V and 0.25V. Timing measurements are made at 1.5V for both a logic "1" and "0."

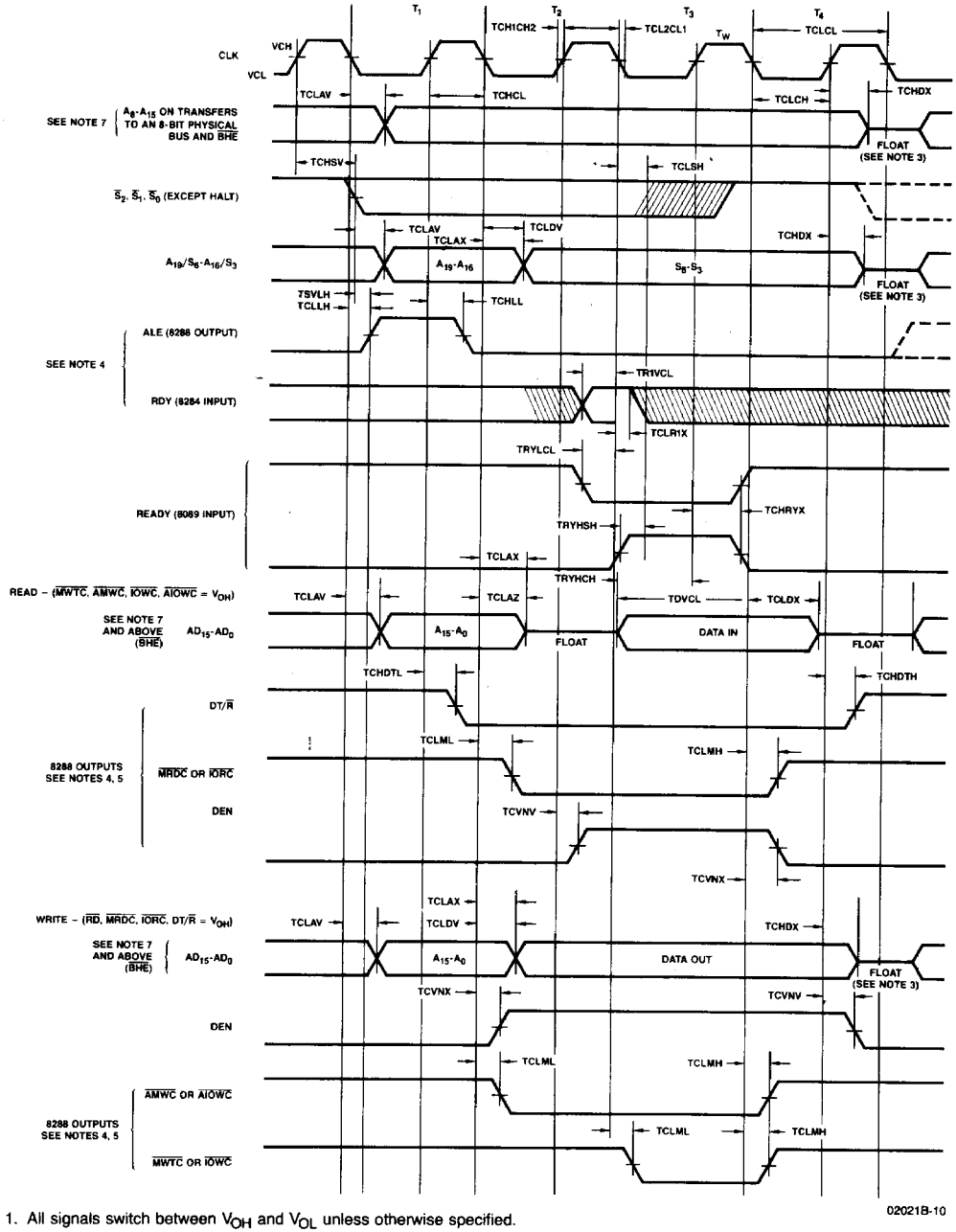
AC TESTING LOAD CIRCUIT



C_L = 100pF
C_L includes jig capacitance

WAVEFORMS

8089 BUS TIMING USING 8288

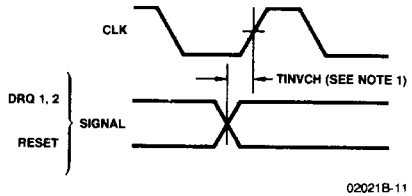


020218-10

Notes:
1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machine states are to be inserted.
3. Following a write cycle data remains valid on the 8089 local bus until a local bus master decides to run another bus cycle. The local bus is floated by the 8089 when the 8089 enters a request bus acknowledge state.
4. Signals at 8284 or 8288 are shown for reference only.
5. The issuance of the 8288 command and control signals ($\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$, and DEN) lags the active high 8288 CEN.
6. All timing measurements are made at 1.5V unless otherwise noted.
7. A_0-A_{15} are stable on transfers to an 8-bit physical data bus i.e., A_8-A_{15} don't float on a read from an 8-bit physical bus or multiplex with data on a write to an 8-bit physical bus $\overline{BHE}$ is stable (non multiplexed) for all transfers.

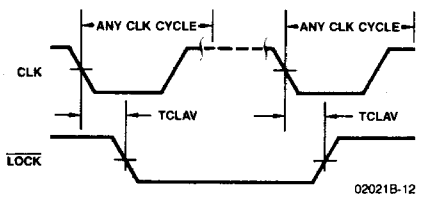
WAVEFORMS (Cont.)

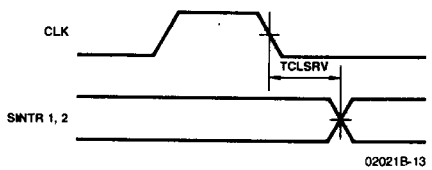
ASYNCHRONOUS SIGNAL RECOGNITION



Notes: 1. Setup requirements for asynchronous signals only to guarantee recognition at next CLK.
2. All inputs except CA are latched on a CLK edge. The CA input is negative edge triggered.
3. DRQ becoming active greater than 30ns after the rising edge of CLK will guarantee non-recognition until the next rising clock edge.

BUS LOCK SIGNAL TIMING AND SINTR





REQUEST/GRANT SEQUENCE